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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,059	06/29/2001	Debashis Bhattacharya	162.7107USU	9475

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EXAMINER	
THOMPSON, ANNETTE M	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/896,059	BHATTACHARYA ET AL.	
	Examiner	Art Unit	
	A. M. Thompson	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-19,21-36,38-44,46-52,54-59 and 61-78* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-19,21-36,38-44,46-52,54-59 and 61-78* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicants' amendment to 09/896,059 has been examined. Claims 1, 11, 12, 21, 22, 30, 31, 32, 39, 40, 47, 48, 54, 55, and 73 are amended. Claim 78 is added. Claims 1-9, 11-19, 21-36, 38-44, 46-52, 54-59, and 61-78 are pending.

1. Applicants' amendment has been fully considered and remarks reviewed. Applicants' amendment is persuasive in part. However, after careful consideration, the pertinent art rejections of the non-final office action are incorporated herein.

Drawings

2. The replacement drawings of Figure 2 is hereby acknowledged and approved.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Rejection of claims 1-9, 11-19, 21-36, 38-44, 46-52, 54-59, and 61-78

4. Claims 1-9, 11-19, 21-36, 38-44, 46-52, 54-59, and 61-78 are rejected under 35 U.S.C. 102(e) as being anticipated by Kumashiro et al., U.S. Patent 6,301,692.

5. Pursuant to claim 1, Kumashiro disclose an automated method for designing integrated circuits (Abstract; col. 1, ll. 14-27), comprising the steps of describing an integrated circuit (Fig. 1, #101; col. 12, ll. 22-23), the description including at least one

design objective of said IC (col. 3, ll. 60-64, wherein the design objective is a reduction in consumed power and an increase in speed for the circuit; col. 4, ll. 3-15, wherein the design objective is to ensure superiority in speed, area and consumed power by a circuit structure); partitioning said description into at least one functional block (fig. 1, #102, circuit dividing processing; col. 12, ll. 24-33); said functional block comprising at least one predefined cell (col. 12, ll. 28-33, the partial circuit); and generating at least one design-specific cell representative of said at least one predefined cell of said functional block (col. 12, ll. 34-40), wherein said design-specific cell is generated, characterized and optimized at the transistor level (col. 14, ll. 1-3; see also col. 13, ll. 48-54; **col. 15, ll. 16-41**) based on said design objective of said IC design (col. 16, ll. 8-13).

6. Pursuant to claim 2, wherein said step of generating comprises evaluating said design-specific cell based on a context of use for said design-specific cell (col. 12, ll. 55-67 to col. 13, line 5 (verifying timing of a given logic circuit based on the register portion delay characteristic library, the partial circuit delay characteristic library, and the net list having the cell level).

7. Pursuant to claim 3, wherein said step of generating comprises characterizing and selecting said design-specific cell from a minimal set comprising at least one cell, based on said IC design objective (Fig. 18, #2102; col. 19, ll. 15-25).

8. Pursuant to claim 4, wherein said step of characterizing and selecting is repeated until the design objective is met (col. 12, ll. 55-67 to col. 2, ll. 1-5; Fig. 1 illustrates an iteration condition at decision box #115.

9. Pursuant to claim 5, wherein said design objective is selected from the group consisting of: IC design die size, die area, performance, power consumption, routability, fault tolerance, signal integrity, testability, reliability and cost (Abstract, last line; col. 21, ll. 1-18).

10. Pursuant to claim 6, further comprising a step of optimizing said IC design (Fig. 1, #111-114; col. 15, ll. 16-25).

11. Pursuant to claim 7, wherein a design metric for the step of optimizing is at least one selected from the group consisting of clock speed, transistor sizing, signal integrity and noise characteristics (col. 7, ll. 25-30 references power consumption and area considerations; col. 15, ll. 22-25 references delay.)

12. Pursuant to claim 8, wherein the optimizing is performed automatically (col. 1, ll. 14-17; Fig. 1 illustrates an automatic process which includes optimizing beginning at #115).

13. Pursuant to claim 9, wherein said optimizing is repeated until said IC design meets at least one design metric (Fig. 1, #114 illustrates the decision step of an iterative optimization).

14. Pursuant to claim 11, Kumashiro discloses a system (Fig. 18; col. 19, ll. 15-27) for implementing an automated integrated circuit design process (Abstract; col. 1, ll. 14-27), said system comprising a description of an integrated circuit (Fig. 1, #101; col. 12, ll. 22-23), the description including at least one design objective of the IC (col. 3, ll. 60-64); a local optimization control for partitioning the description into at least one functional block (fig. 1, #102, the circuit dividing processing provides a local optimization

control function; col. 12, ll. 24-33), the functional block comprising at least one predefined cell (col. 12, ll. 28-33, the partial circuit); and a design-specific generator (the main cell layout generating processing performs this function, col. 17, ll. 23-29; see also col. 12, ll. 34-40) for generating at least one design specific cell representation of the at least one defined cell the functional block wherein said design-specific cell is generated, characterized and optimized at the transistor level (col. 14, ll. 1-3; see also col. 13, ll. 48-54; **col. 15, ll. 16-41**)based on the design objective of the IC (col. 16, ll. 8-13).

15. Pursuant to claims 12-19, these claims incorporate the limitations already rejected in claims 2-9, respectively, supra, and are likewise rejected here based on the same reasoning.

16. Pursuant to claims 21-29, these claims recite the steps of the method already rejected in claims 1-9, respectively, and therefore claims 21-29 are rejected here based on the same reasoning.

17. Pursuant to claims 30, 62-69, these claims recites a storage medium with computer readable program instructions for automatically designing an IC using the claimed method of claims 1-9, respectively, supra. Kumashiro also discloses the limitation of a storage medium with computer readable instructions in claims 26, 27, and additionally at col. 25, ll. 9-13. Therefore, claims 30 and 62-69 are likewise rejected based on the reasoning provided in the rejections of claims 1-9, respectively.

18. Pursuant to claim 31, this claim incorporates limitations already rejected in claims 1 and 6, and is likewise rejected based on the same rejection reasoning.

19. Pursuant to claims 32-35, these claims incorporate limitations already rejected in claims 2-5, supra, and are likewise rejected based on the same reasoning.

20. Pursuant to claim 36, these claims incorporate limitations already rejected in claim 7, supra, and is likewise rejected here based on the same reasoning.

21. Pursuant to claim 38, wherein said design-specific cell is a transistor-level cell (Figs. 4A, 4B, col. 13, line 55 to col. 14, line 8).

22. Pursuant to claim 39, this claim incorporates the limitations of claims 1 and 9, rejected, supra, and therefore claim 39 is likewise rejected here based on the same reasoning.

23. Pursuant to claims 40-43, these claims incorporate the limitations of claims 2-5, rejected, supra, and are likewise rejected here based on the same reasoning.

24. Pursuant to claim 44, this claim incorporates the limitations of claim 7, rejected, supra, and is likewise rejected here based on the same reasoning.

25. Pursuant to claim 46, this claim incorporates the limitation of claim 38, rejected, supra, and is likewise rejected here based on the same reasoning.

26. Pursuant to claim 47, this claim incorporates the limitation of claims 1 and 9, rejected supra, and therefore claim 47 is likewise rejected here based on the same reasoning.

27. Pursuant to claims 48-52, these claims incorporate the limitations of claims 2-5 and 7, rejected supra, and therefore claims 48-52 are likewise respectively rejected based on the same reasoning.

28. Pursuant to claim 54, this claim incorporates the limitations of claims 1 and 9, rejected, supra, and therefore claim 39 is likewise rejected here based on the same reasoning.

29. Pursuant to claims 55-59, these claims incorporate the limitations of claims 2-5 and 7, rejected supra, and therefore claims 55-59 are likewise rejected here based on the same reasoning.

30. Pursuant to claim 61, this claim incorporates the limitation of claim 38, rejected, supra, and is likewise rejected here based on the same reasoning.

31. Pursuant to claims 70-77 wherein said design specific cell is at least on selected from the group consisting of CMOS cells, static CMOS cells, and dynamic CMOS cells (col. 15, ll. 26-36; col. 19, ll. 15-59).

32. Pursuant to claim 78, wherein said design-specific cell is optimized at the transistor level for at least one selected from the group consisting of: performance, area, power consumption, testability and fault tolerance (col. 15, ll. 16-41, wherein the optimization is for performance).

Remarks

33. After further consideration the following determinations were made:

a) Kumashiro generates a partial circuit at the transistor level (col. 12, ll. 34-45). Further, Kumashiro optimizes at the transistor level prior to the layout processing (col. 15, ll. 16-25). Additionally, Kumashiro partitions the IC design into at least one functional block; col. 12, ll. 22-28 discloses a circuit that is partitioned into a combinational circuit portion and a register portion.

34. Recalling Applicants' personal interview which included a PowerPoint demonstration, Examiner believes that Applicants' invention has novelty. Nevertheless, the claim language continues to read on Kumashiro and Examiner has no suggestions that will assist Applicant in overcoming the instant rejection.

Conclusion

35. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

36. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m..

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

37. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)

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